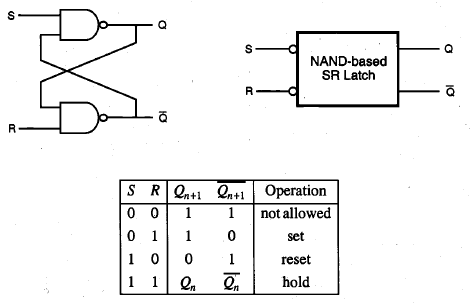
**Circuit Diagram & Truth Table:**

****

**Diagram

Description automatically generated**

**Code:**

* **Design Module**

modulesrff(q,qb,r,s,clk);

inputr,s,clk;

outputq,qb;

wirea,b;

nand a1(a,r,clk);

nand a2(b,s,clk);

nand n1(q,a,qb);

nand n2(qb,b,q);

endmodule

* **TestBench**

module tb;

regr,s,clk;

wireq,qb;

srff r1(q,qb,r,s,clk);

initial

clk=1'b0;

always #30

clk=~clk;

initial

begin

r=1'b0;s=1'b0;

#30

r=1'b1;s=1'b0;

#30

r=1'b0;s=1'b1;

#30

r=1'b1;s=1'b1;

#30

$finish;

end

endmodule